

# DATA SHEET

## **74LVC245A; 74LVCH245A**

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

Product specification  
Supersedes data of 2002 Jun 20

2003 May 07

## Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

## 74LVC245A; 74LVCH245A

### FEATURES

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when  $V_{CC} = 0$  V
- bus-hold on all data inputs (74LVCH245A only)
- Complies with JEDEC standard no. 8-1A
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from  $-40$  to  $+85$  °C and  $-40$  to  $+125$  °C.

### DESCRIPTION

The 74LVC245A/74LVCH245A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation outputs can handle 5 V. These features allow the use of these devices as translators in a mixed 3.3 and 5 V environment.

The 74LVC245A/74LVCH245A is an octal transceiver with non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74LVC245A/74LVCH245A has an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) input for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ , $B_n$ to $A_n$	$C_L = 50$ pF; $V_{CC} = 3.3$ V	2.9	ns
$C_I$	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		10.0	pF
$C_{PD}$	power dissipation capacitance per buffer	$V_{CC} = 3.3$ V; notes 1 and 2	15	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND to } V_{CC}$ .

Octal bus transceiver with direction pin with 5 V tolerant  
input/outputs (3-state)74LVC245A;  
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## ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVC245AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVCH245AD	-40 to +125 °C	20	SO20	plastic	SOT163-1
74LVC245ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVCH245ADB	-40 to +125 °C	20	SSOP20	plastic	SOT339-1
74LVC245APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVCH245APW	-40 to +125 °C	20	TSSOP20	plastic	SOT360-1
74LVC245ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1
74LVCH245ABQ	-40 to +125 °C	20	DHVQFN20	plastic	SOT764-1

## FUNCTION TABLE

See note 1.

INPUT		INPUT/OUTPUT	
$\overline{\text{OE}}$	DIR	$A_n$	$B_n$
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

## Note

- H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
Z = high-impedance OFF-state.

## PINNING

PIN	SYMBOL	DESCRIPTION
1	DIR	direction control input
2	$A_0$	data input/output
3	$A_1$	data input/output
4	$A_2$	data input/output
5	$A_3$	data input/output
6	$A_4$	data input/output
7	$A_5$	data input/output
8	$A_6$	data input/output
9	$A_7$	data input/output
10	GND	ground (0 V)

PIN	SYMBOL	DESCRIPTION
11	$B_7$	data input/output
12	$B_6$	data input/output
13	$B_5$	data input/output
14	$B_4$	data input/output
15	$B_3$	data input/output
16	$B_2$	data input/output
17	$B_1$	data input/output
18	$B_0$	data input/output
19	$\overline{\text{OE}}$	output enable input (active LOW)
20	$V_{CC}$	supply voltage

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

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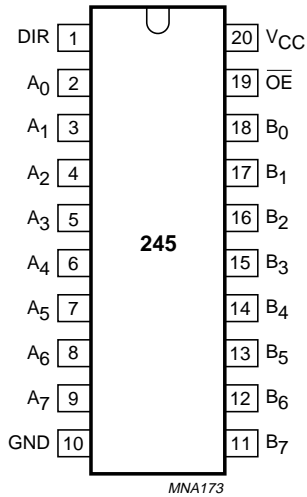
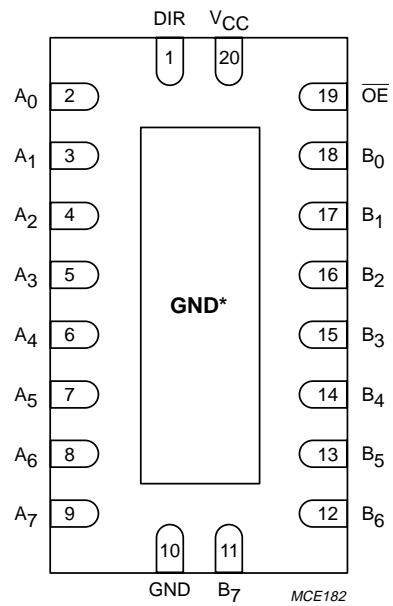


Fig.1 Pin configuration SO20 and (T)SSOP20.



\* The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN20.

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

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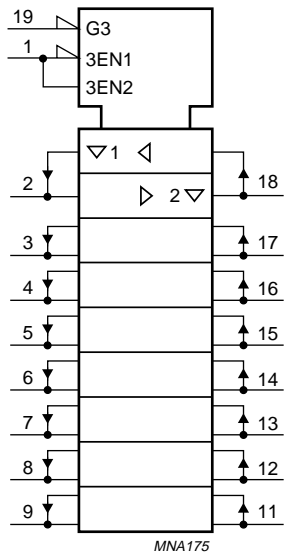


Fig.3 Logic symbol (IEEE/IEC).

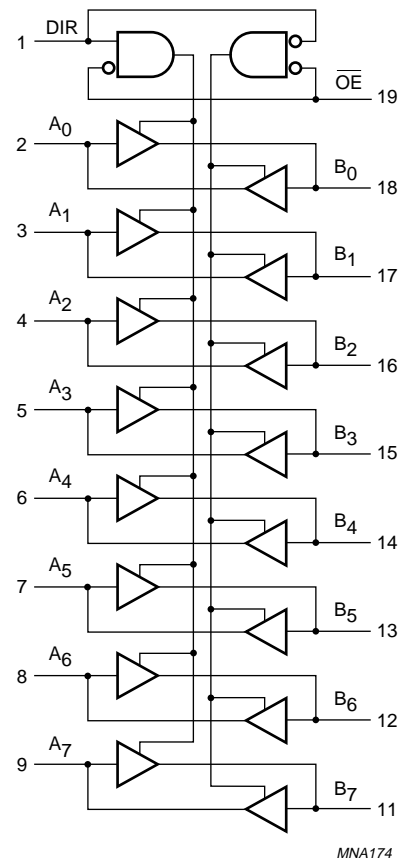


Fig.4 Logic symbol.

Octal bus transceiver with direction pin with 5 V tolerant  
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**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	for maximum speed performance	2.7	3.6	V
		for low-voltage applications	1.2	3.6	V
V <sub>I</sub>	input voltage		0	5.5	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
		output 3-state	0	5.5	V
T <sub>amb</sub>	operating ambient temperature		-40	+125	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall times	V <sub>CC</sub> = 1.2 to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 to 3.6 V	0	10	ns/V

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+6.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0	-	-50	mA
V <sub>I</sub>	input voltage	note 1	-0.5	+6.5	V
I <sub>OK</sub>	output diode current	V <sub>O</sub> > V <sub>CC</sub> or V <sub>O</sub> < 0	-	±50	mA
V <sub>O</sub>	output voltage	output HIGH or LOW state; note 1	-0.5	V <sub>CC</sub> + 0.5	V
		output 3-state; note 1	-0.5	+6.5	V
I <sub>O</sub>	output source or sink current	V <sub>O</sub> = 0 to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 to +125 °C; note 2	-	500	mW

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. For SO20 packages: above 70 °C derate linearly with 8 mW/K.  
For SSOP20 and TSSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.  
For DHVQFN20 packages: above 60 °C derate linearly with 4.5 mW/K.

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## DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	-	-	V
			2.7 to 3.6	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		1.2	-	-	0	V
			2.7 to 3.6	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA I <sub>O</sub> = -12 mA I <sub>O</sub> = -18 mA I <sub>O</sub> = -24 mA	2.7 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
			2.7	V <sub>CC</sub> - 0.5	-	-	V
			3.0	V <sub>CC</sub> - 0.6	-	-	V
			3.0	V <sub>CC</sub> - 0.8	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA I <sub>O</sub> = 12 mA I <sub>O</sub> = 24 mA	2.7 to 3.6	-	0	0.2	V
			2.7	-	-	0.4	V
			3.0	-	-	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; note 2	3.6	-	±0.1	±5	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; notes 2 and 3	3.6	-	±0.1	±5	µA
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	-	±0.1	±10	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	-	0.1	10	µA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	-	5	500	µA
I <sub>BH(L)</sub>	bus-hold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4, 5 and 6	3.0	75	-	-	µA
I <sub>BH(H)</sub>	bus-hold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4, 5 and 6	3.0	-75	-	-	µA
I <sub>BH(LO)</sub>	bus-hold LOW overdrive current	notes 4, 5 and 7	3.6	500	-	-	µA
I <sub>BH(HO)</sub>	bus-hold HIGH overdrive current	notes 4, 5 and 7	3.6	-500	-	-	µA

Octal bus transceiver with direction pin with 5 V tolerant  
input/outputs (3-state)74LVC245A;  
74LVCH245A

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.2	V <sub>CC</sub>	–	–	V
			2.7 to 3.6	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.2	–	–	0	V
			2.7 to 3.6	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 µA I <sub>O</sub> = -12 mA I <sub>O</sub> = -18 mA I <sub>O</sub> = -24 mA	2.7 to 3.6	V <sub>CC</sub> - 0.3	–	–	V
			2.7	V <sub>CC</sub> - 0.65	–	–	V
			3.0	V <sub>CC</sub> - 0.75	–	–	V
			3.0	V <sub>CC</sub> - 1	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 µA I <sub>O</sub> = 12 mA I <sub>O</sub> = 24 mA	2.7 to 3.6	–	–	0.3	V
			2.7	–	–	0.6	V
			3.0	–	–	0.8	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND; note 2	3.6	–	–	±20	µA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5 V or GND; notes 2 and 3	3.6	–	–	±20	µA
I <sub>off</sub>	power off leakage supply	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0.0	–	–	±20	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	3.6	–	–	40	µA
ΔI <sub>CC</sub>	additional quiescent supply current per in. pin	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0	2.7 to 3.6	–	–	5000	µA
I <sub>BH(L)</sub>	bus-hold LOW sustaining current	V <sub>I</sub> = 0.8 V; notes 4, 5 and 6	3.0	60	–	–	µA
I <sub>BH(H)</sub>	bus-hold HIGH sustaining current	V <sub>I</sub> = 2.0 V; notes 4, 5 and 6	3.0	-60	–	–	µA
I <sub>BH(LO)</sub>	bus-hold LOW overdrive current	notes 4, 5 and 7	3.6	500	–	–	µA
I <sub>BH(HO)</sub>	bus-hold HIGH overdrive current	notes 4, 5 and 7	3.6	-500	–	–	µA

**Notes**

- All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
- For bus-hold parts, the bus-hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input terminal.
- For I/O ports the parameter I<sub>OZ</sub> includes the input leakage current.
- Valid for data inputs of bus-hold parts (74LVCH245A) only.
- For data inputs only, control inputs do not have a bus-hold circuit.
- The specified sustaining current at the data input holds the input below the specified V<sub>I</sub> level.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.



Octal bus transceiver with direction pin with 5 V tolerant  
input/outputs (3-state)74LVC245A;  
74LVCH245A

## AC CHARACTERISTICS

GND = 0 V;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> , B <sub>n</sub> to A <sub>n</sub>	see Figs 5 and 7	1.2	–	17	–	ns
			2.7	1.5	3.4	7.3	ns
			3.0 to 3.6	1.5	2.9 <sup>(1)</sup>	6.3	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> , OE to B <sub>n</sub>	see Figs 6 and 7	1.2	–	22	–	ns
			2.7	1.5	5.0	9.5	ns
			3.0 to 3.6	1.5	4.0 <sup>(1)</sup>	8.5	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> , OE to B <sub>n</sub>	see Figs 6 and 7	1.2	–	12	–	ns
			2.7	1.5	3.6	8.0	ns
			3.0 to 3.6	1.7	3.4 <sup>(1)</sup>	7.0	ns
t <sub>sk(0)</sub>	skew	note 2		–	–	1.0	ns
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> , B <sub>n</sub> to A <sub>n</sub>	see Figs 5 and 7	1.2	–	–	–	ns
			2.7	1.5	–	9.5	ns
			3.0 to 3.6	1.5	–	8.0	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time OE to A <sub>n</sub> , OE to B <sub>n</sub>	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	12.0	ns
			3.0 to 3.6	1.5	–	11.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time OE to A <sub>n</sub> , OE to B <sub>n</sub>	see Figs 6 and 7	1.2	–	–	–	ns
			2.7	1.5	–	10.0	ns
			3.0 to 3.6	1.7	–	9.0	ns
t <sub>sk(0)</sub>	skew	note 2		–	–	1.5	ns

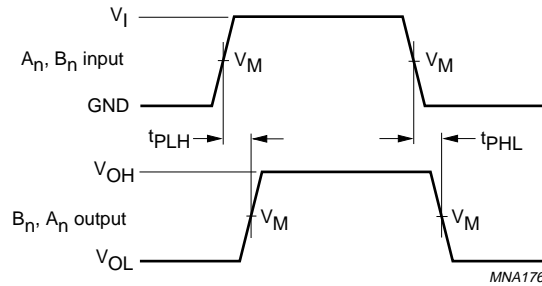
## Notes

1. Typical values are measured at V<sub>CC</sub> = 3.3 V.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

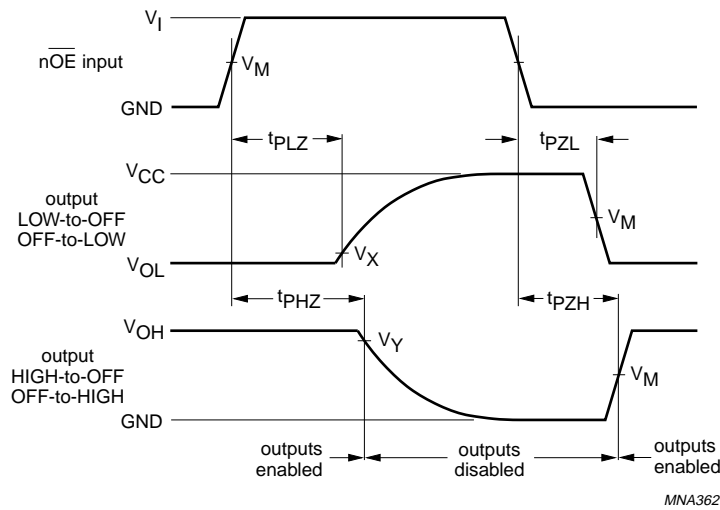
74LVC245A;  
74LVCH245A

AC WAVEFORMS



$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ .  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ .  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.5 The inputs  $A_n$ ,  $B_n$  to outputs  $B_n$ ,  $A_n$  propagation delays.



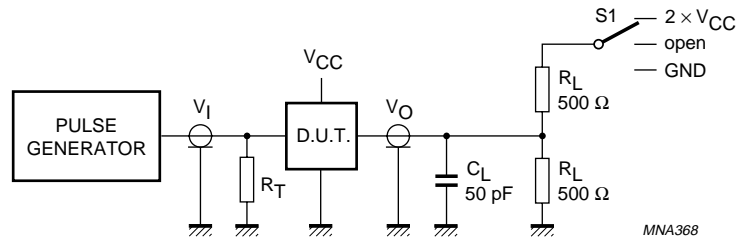
$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_M = 0.5V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_X = V_{OL} + 0.1\text{ V}$  at  $V_{CC} < 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.3\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;  
 $V_Y = V_{OH} - 0.1\text{ V}$  at  $V_{CC} < 2.7\text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

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SWITCH POSITION	
TEST	SWITCH
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	$V_I$
$< 2.7 \text{ V}$	$V_{CC}$
$2.7 - 3.6 \text{ V}$	$2.7 \text{ V}$

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.7 Load circuitry for switching times.

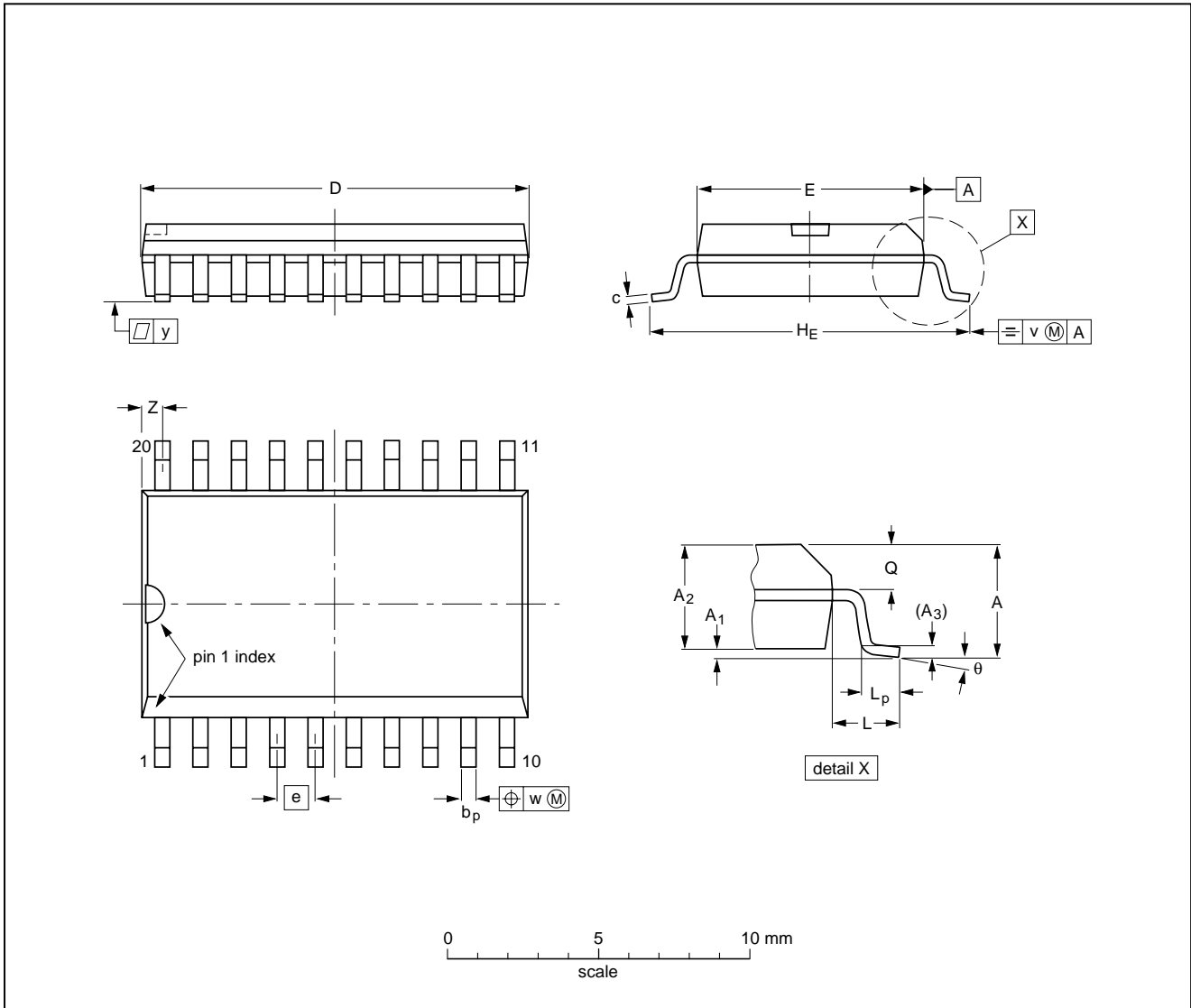
Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

74LVC245A;  
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PACKAGE OUTLINES

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

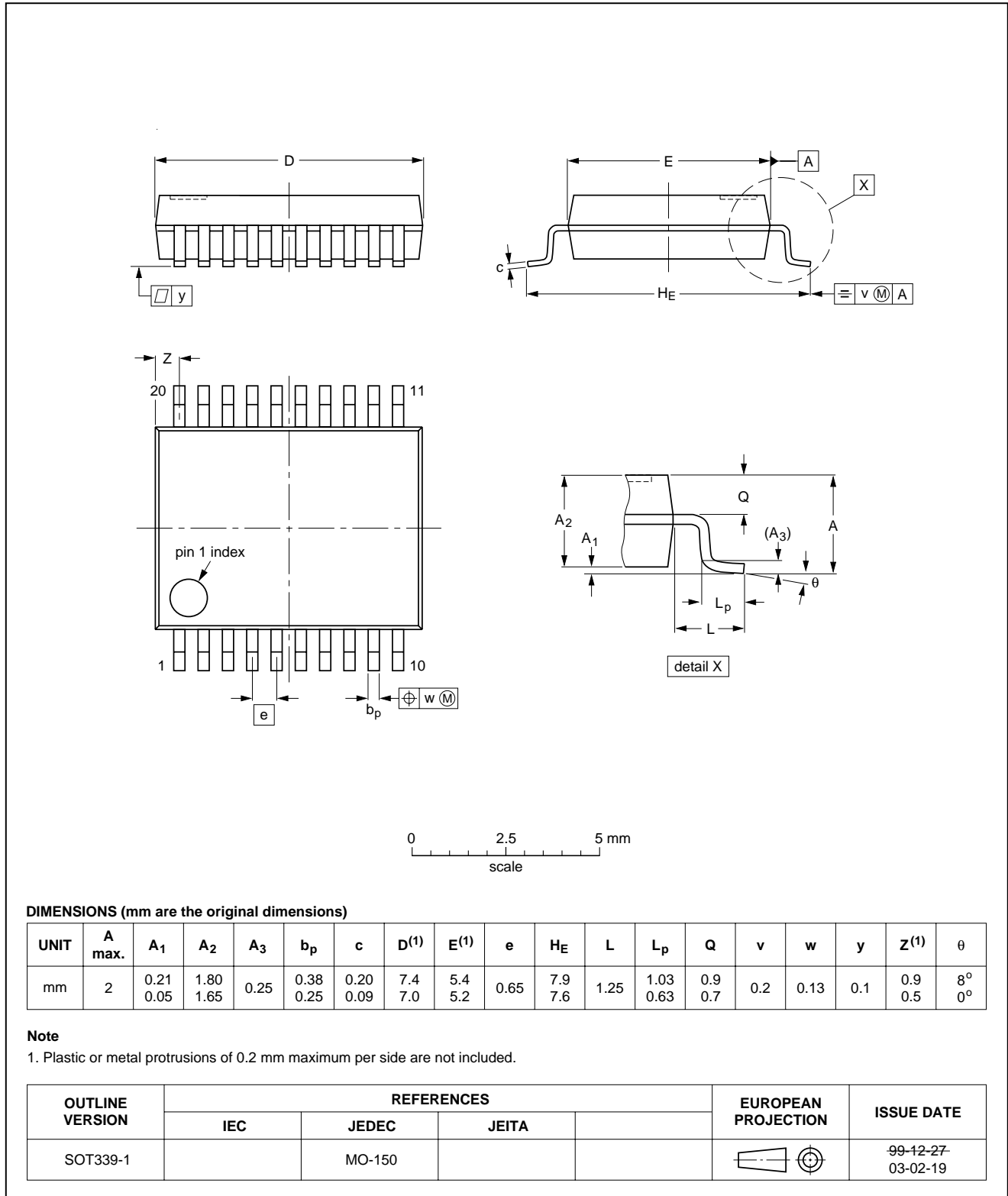
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

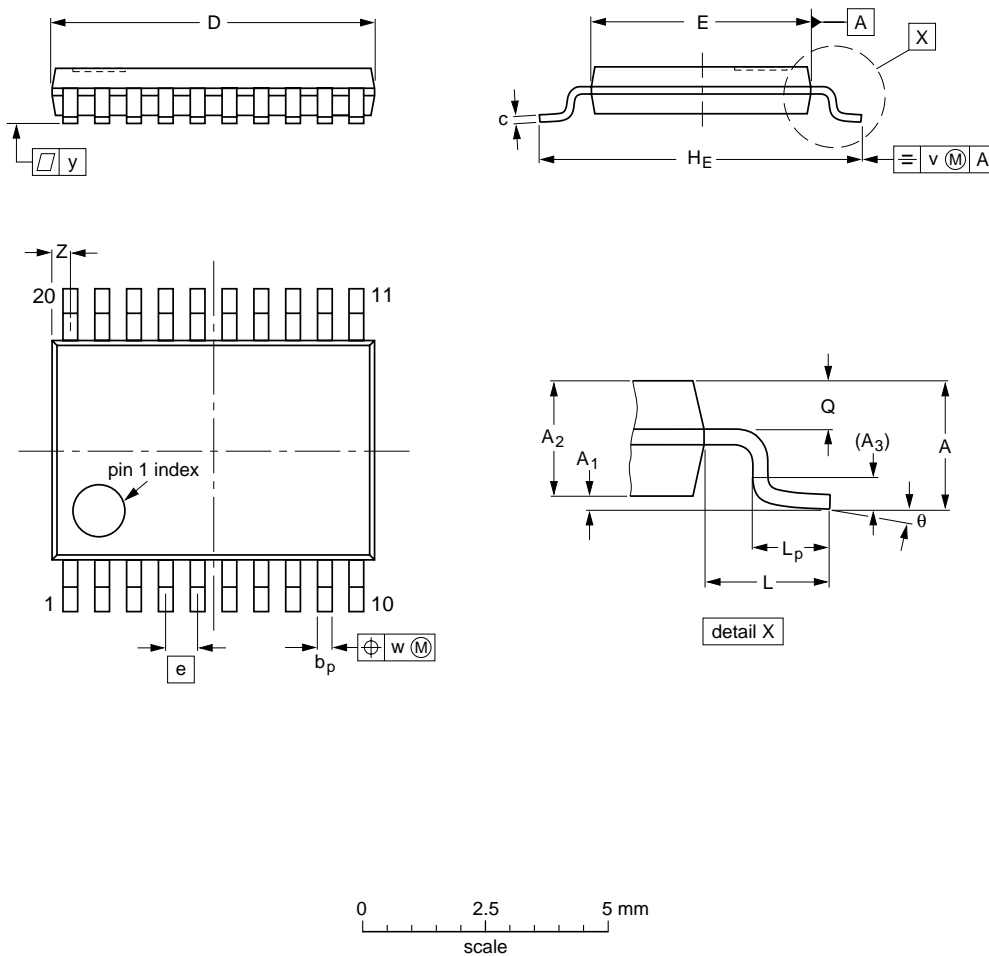


Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

74LVC245A;  
74LVCH245A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

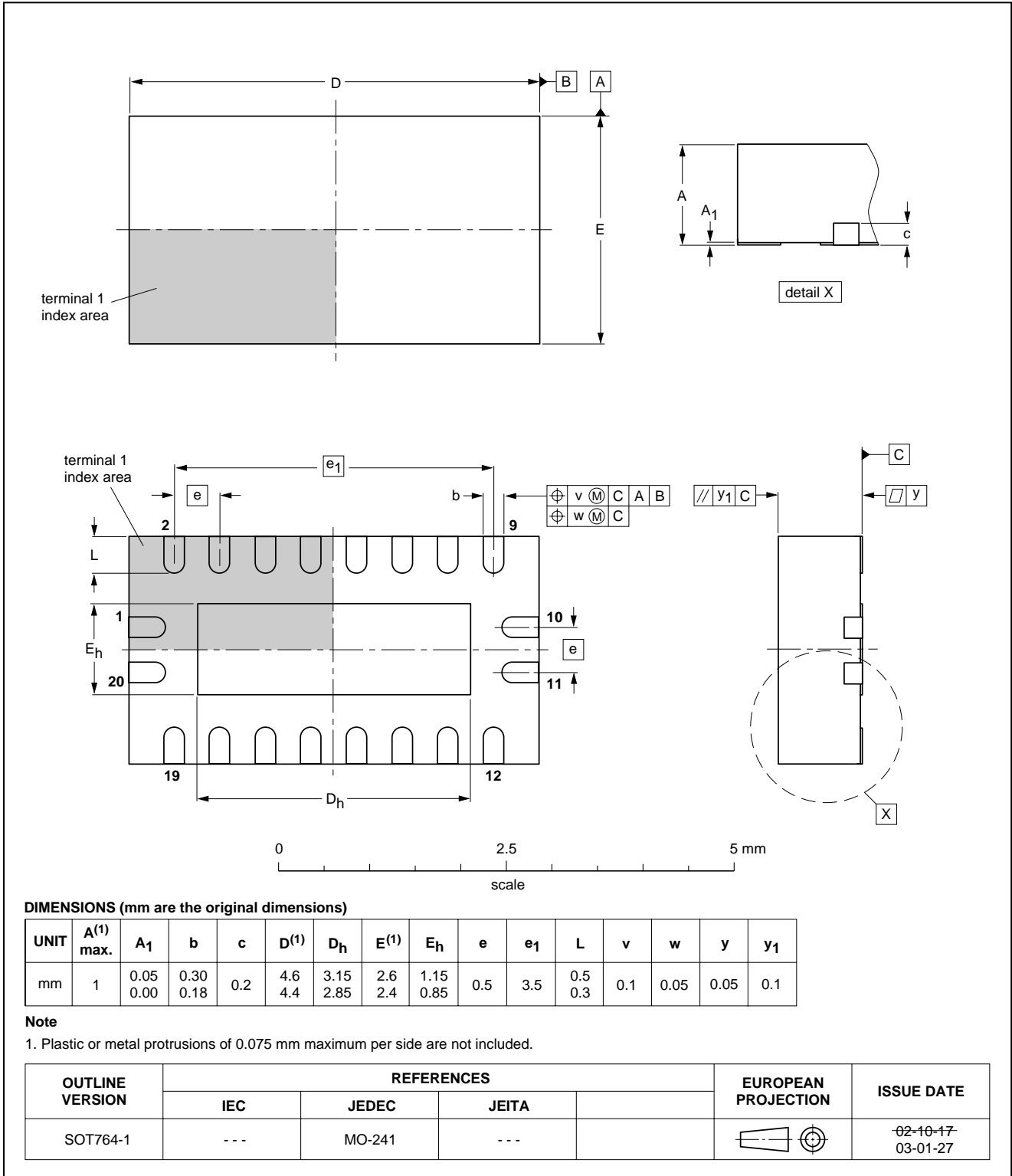
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				99-12-27- 03-02-19

Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

74LVC245A;  
74LVCH245A

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1



## Octal bus transceiver with direction pin with 5 V tolerant input/outputs (3-state)

74LVC245A;  
74LVCH245A

### SOLDERING

#### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

#### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept:

- below 220 °C for all the BGA packages and packages with a thickness  $\geq 2.5$  mm and packages with a thickness  $< 2.5$  mm and a volume  $\geq 350$  mm<sup>3</sup> so called thick/large packages
- below 235 °C for packages with a thickness  $< 2.5$  mm and a volume  $< 350$  mm<sup>3</sup> so called small/thin packages.

#### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

#### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.



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#### Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE <sup>(1)</sup>	SOLDERING METHOD	
	WAVE	REFLOW <sup>(2)</sup>
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable <sup>(3)</sup>	suitable
PLCC <sup>(4)</sup> , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended <sup>(4)(5)</sup>	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended <sup>(6)</sup>	suitable

#### Notes

- For more detailed information on the BGA packages refer to the “(LF)BGA Application Note” (AN01026); order a copy from your Philips Semiconductors sales office.
- All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
- These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
- If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
- Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
- Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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#### DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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**NOTES**

# *Philips Semiconductors – a worldwide company*

## **Contact information**

For additional information please visit <http://www.semiconductors.philips.com>. Fax: +31 40 27 24825  
For sales offices addresses send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

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